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AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A fixed point data generating circuit which receives a plurality of floating point data and converts said received plurality of floating point data into respective fixed point data, said fixed point data generating circuit comprising:

a reference data determining unit for determining a reference floating point data from said received plurality of floating point data;

an exponent part subtractor unit for obtaining the differences between the values of the exponent parts of the received floating point data which are not determined as said reference floating point data and a value of an exponent part of said reference floating point data;

a shifting unit for shifting a mantissa part of each of said plurality of floating point data by the difference obtained for the corresponding floating point data; and

a bit extracting unit for extracting a predetermined number of bits of each shifted mantissa part as fixed point data, a leading bit of said predetermined number of bits comprising a second bit from the most significant bit (MSB) of the shifted bits except the sign bit,

wherein when an overflow occurs in said extracted bits, said bit extracting unit outputs a predetermined maximum value of said fixed point data ~~bits extracted by said bit extracting unit as said fixed point data, said extracted bits are accepted as representing the maximum value~~.

2. (Previously presented) A fixed point data generating circuit as set forth in claim 1, wherein said reference data determining unit comprises a maximum value detecting circuit which detects the maximum value from among the values of said plurality of floating point data, and said reference floating point data is the data having the detected maximum value.

3. (Previously presented) A fixed point data generating circuit as set forth in claim 1, wherein said reference data determining unit comprises a minimum value detecting circuit which detects the minimum value from among the values of said plurality of floating point data, and said reference floating point data is the data having the detected minimum value.

4. (Previously presented) A fixed point data generating circuit as set forth in claim 1, wherein said reference data determining unit comprises an average value calculating circuit which calculates an average value of the values of said floating point data, and said reference floating point data is data having the average value.

5-9. (Canceled)

10. (Currently amended) A computer-implemented method for performing Viterbi decoding utilizing fixed point data obtained by converting a plurality of inputted floating point data into respective fixed point data, said computer-implemented method comprising:

determining a reference floating point data from said plurality of inputted floating point data;

obtaining the differences between the values of the exponent parts of the inputted floating point data which are not determined as said reference floating point data and a value of an exponent part of said reference floating point data;

shifting a mantissa part of each of said plurality of floating point data by the difference obtained for the corresponding floating point data;

extracting a predetermined number of bits of each shifted mantissa part as fixed point data, a leading bit of said predetermined number of bits comprising a second bit from the most significant bit (MSB) of the shifted bits except the sign bit; and

inputting said fixed point data to a Viterbi decoder to perform ~~performing~~ Viterbi decoding with the fixed point data,

wherein in extracting the predetermined number of bits, when an overflow occurs in

said extracted bits, a predetermined maximum value of said fixed point data is output ~~said extracted bits are accepted as representing the maximum value~~.

11. (Original) A method for generating fixed point data as set forth in claim 10, wherein said reference floating point data is the maximum data among said plurality of floating point data.

12. (Original) A method for generating fixed point data as set forth in claim 10, wherein said reference floating point data is the minimum data among said plurality of floating point data.

13. (Previously presented) A method for generating fixed point data as set forth in claim 10, wherein said reference floating point data is the average data of said plurality of floating point data.

14-18. (Canceled)

19. (Previously presented) A method for generating fixed point data as set forth in claim 10, further comprising utilizing the fixed point data.

20. (Previously presented) A method for generating fixed point data as set forth in claim 19, wherein the fixed point data is utilized in a Code Division Multiple Access system.

21. (Currently amended) A Viterbi decoding method, comprising:

receiving a first floating point data;

shifting a mantissa part of said first floating point data;

extracting a predetermined number of bits of said shifted mantissa part ~~of a mantissa of said first floating point data~~ as a fixed point data, said fixed point data being utilized in a

Viterbi decoding, a leading bit of said extracted bits comprising a second bit from the most significant bit (MSB) of the shifted bits except the sign bit;

saturating said fixed point data when, in said mantissa of said first floating point data, a more significant bit than said part extracted as said fixed point data is 1; and

inputting said fixed point data to a Viterbi decoder to perform ~~performing~~ a Viterbi decoding by utilizing said fixed point data,

wherein in said extracting said predetermined number of bits, when an overflow occurs in said extracted bits, a predetermined maximum value of said fixed point data is output.

22. (Previously presented) The Viterbi decoding method according to claim 21, wherein said saturating said fixed point data comprises saturating said fixed point data except a sign bit.

23. (Previously presented) The Viterbi decoding method according to claim 22, wherein said sign bit comprises a most significant bit of said fixed point data.

24. (Previously presented) The Viterbi decoding method according to claim 21, wherein a location, in said mantissa of said first floating point data, of said part extracted as said fixed data is determined to improve a decoding rate of said Viterbi decoding.

25. (Previously presented) The Viterbi decoding method according to claim 22, further comprising:

receiving a plurality of floating point data;

determining a reference floating point data from said plurality of received floating point data;

obtaining a difference between values of exponent parts of the received floating point data which are not determined as said reference floating point data and a value of an exponent

part of said reference floating point data; and

shifting a mantissa part of each of said plurality of floating point data by the difference obtained for the corresponding floating point data in order to generate said first floating point data.

26. (Previously presented) The Viterbi decoding method according to claim 25, wherein said reference floating point data comprises a maximum value among said plurality of floating point data.

27. (Previously presented) The Viterbi decoding method according to claim 25, wherein said reference floating point data comprises a minimum value among said plurality of floating point data.

28. (Previously presented) The Viterbi decoding method according to claim 25, wherein said reference floating point data comprises an average value of said plurality of floating point data.